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TITLE: DEVICE AND METHOD FOR I/Q MODULATION, FREQUENCY TRANSLATION AND UPSAMPLING

Technical Field

The present invention relates generally to network interfacing, and more particularly, to a device and method for I/Q modulation, frequency translation, upsampling, and pulse shaping.

Background of the Invention

The transmission of various types of digital data between computers continues to grow in importance. The predominant method of transmitting such digital data includes coding the digital data into a low frequency base data signal and modulating the base data signal onto a high frequency carrier signal. The high frequency carrier signal is then transmitted across a network cable medium, via RF signal, modulated illumination, or other network medium, to a remote network node.

At the remote computing station, the high frequency carrier signal must be received and demodulated to recover the original base data signal. In the absence of any distortion of the carrier signal across the network medium, the received carrier would be identical in phase, amplitude, and frequency to the transmitted carrier and could be demodulated using known mixing techniques to recover the base data signal. The base data signal could then be recovered into digital data using known sampling algorithms.

One problem with such networks is that the network topology tends to distort the high frequency carrier signal due to numerous branch connections and different lengths of such branches causing numerous reflections of the transmitted carrier. The high frequency carrier is further distorted by spurious noise caused by electrical devices operating in close proximity to the cable medium. Such problems are even more apparent in a network which uses home telephone wiring cables as the network cable medium because the numerous branches and connections are typically designed for transmission of plain old telephone system (POTS) signals in the 3-10 kilohertz frequency and are not designed for transmission of high frequency carrier signals on the order of 7

Megahertz. Further yet, the high frequency carrier signal is further distorted by turn-on transients due to on-hook and off-hook noise pulses of the POTS utilizing the network cables.

Such distortion of frequency, amplitude, and phase of the high frequency carrier signal degrades network performance and tends to impede the design of higher data rate networks. Known techniques for compensating for such distortion and improving the data rate of a network include complex modulation schemes.

Utilizing a complex modulation scheme such as quadrature amplitude modulation (QAM) data, both the amplitude and phase of the high frequency carrier are modulated to represent I and Q components of a base data signal. Referring to Figure 1, a 4-QAM modulation constellation 10 is shown. In operation, each data symbol is represented by an I-value of +1 or –1 and a Q-value of +1 or –1 such that the data symbol can be represented by one of the four modulation states 12(a) – (d) in constellation 10. Each constellation state 12(a) – 12(d) represents a unique combination of carrier amplitude and phase. For example, constellation state 12(a) represents a carrier amplitude of 14 and a carrier phase 16.

A complex modulation transmitter typically uses a look up table to generate an I-channel and a Q-channel baud rate data signal. An upsampler then inserts additional sample values of zero to increase the input sample frequency to a frequency greater than the desired carrier frequency. A complex mixer then mixes each of the I-channel signal and the Q-channel signal by digital sine waves and digital cosine waves of the carrier frequency as appropriate to generate a modulated carrier signal. Narrow band digital filters are then used to remove harmonics and to assure that the transmitted signal has a strong signal to noise ratio within the desired band without excessive noise in the side bands.

A problem with such systems is that a carrier frequency on the order of 7MHz is typically represented by digital values clocked at a frequency on the order of 32MHz. As such, a digital signal processor (DSP) implementation of a QAM (or I/Q) transmitter can consume many gates or may not even be possible to

implement in a high speed DSP without architectural innovation. What is needed is a device and method for I/Q modulation, upsampling, and digital filtering that does not suffer the disadvantages of known systems.

Summary of the Invention

A first aspect of the present invention is to provide a device for modulating a carrier signal which simultaneously performs frequency translation, upsampling, and pulse shaping. The device comprises: (a) a mapper generating a first data signal at a selected one of a plurality of baud rates; (b) a scaler multiplying the first data signal by one of a plurality of predetermined scaler values selected to correspond to the baud rate to generate a scaled data signal; (c) a complex mixer for generating a frequency shifting scaled data signal; (d) an upsampler circuit for increasing the sampling frequency of the frequency shifted scaled data signal; and (e) a pulse shaper circuit for generating a digital representation of a modulated carrier signal in accordance with the frequency shifted scaled data signal.

The first data signal may comprise an I-channel first data signal and a Q-channel first data signal. Similarly, the scaled data signal may comprise an I-channel scaled data signal and a Q-channel scaled data signal, and the frequency shifted scaled data signal may comprise and I-channel frequency shifted scaled data signal and a Q-channel frequency shifted scaled data signal.

The first data signal may be a digital data signal with a sampling frequency corresponding to the highest of the plurality of baud rates and each of the predetermined scaler values is a value which provides for the scaled data signal to have approximately the same signal strength independent of baud rate. In the exemplary embodiment, the plurality of baud rates includes 2 Mbaud and 4 Mbaud, the sampling rate is 4MHz, and the predetermined scaler values are a value of 1 corresponding to the 2 Mbaud baud rate and a value of 2/3 corresponding to the 4 Mbaud baud rate.

The complex mixer may include a first and a second multiplier each multiplying the I-channel scaled data signal by a sine waveform and a cosine

waveform respectively, and a third and fourth multiplier each multiplying the Q-channel scaled data signal by the sine waveform and a cosine waveform respectively. A first summer adds the result of the second multiplier to the result of the third multiplier, multiplied by negative one, to generate the I-channel frequency shifted scaled data signal and a second channel summer adds the result of the first multiplier and the result of the fourth multiplier to generate the Q-channel frequency shifted scaled data signal. In the exemplary embodiment, the sine waveform and the cosine waveform each have a frequency of one fourth the sampling frequency.

The pulse shaper circuit may include a finite impulse response filter and a coefficient matrix storing a set of coefficients for each of the I-channel and the Q-channel. The finite impulse response filter may include 16-tap finite impulse filter and each set of filter coefficients includes nine non-zero coefficients with each coefficient being a 10-bit coefficient.

A second aspect of the present invention is to provide a method for modulating a carrier signal. The method comprises: (a) generating a first data signal at a selected one of a plurality of baud rates; (b) scaling the first data signal by one of a plurality of predetermined scaler values selected to correspond to the baud rate to generate a scaled data signal; (c) mixing the scaled data signal with a frequency signal to generate a frequency shifted scaled data signal; (d) increasing the sampling frequency of the frequency shifted scaled data signal; and (e) filtering the frequency shifted scaled data signal to generate a digital representation of a modulated carrier signal.

The step of generating the first data signal may comprise generating both an I-channel first data signal and a Q-channel first data signal. Similarly, the step of scaling the first data signal may comprise scaling the I-channel first data signal and the Q-channel first data signal and the step of mixing the scaled data signal may include complex mixing of both the I-channel scaled data signal and the Q-channel scaled data signal.

The first data signal may be a digital data signal with a sampling frequency corresponding to the highest of the plurality of baud rates and each of the

predetermined scaler values is a value which provides for the scaled data signal to have approximately the same signal strength independent of baud rate. In the exemplary embodiment, the plurality of baud rates includes 2 Mbaud and 4 Mbaud, the sampling rate is 4MHz, and the predetermined scaler values are a value of 1 corresponding to the 2 Mbaud baud rate and a value of 2/3 corresponding to the 4 Mbaud baud rate.

The step of complex mixing the scaled data signal may include: (i) subtracting the result of the Q-channel scaled data signal multiplied by a sine waveform from the result of the I-channel scaled data signal multiplied by a cosine waveform to generate an I-channel frequency shifted data signal; and (ii) adding the result of the Q-channel scaled data signal multiplied by a cosine waveform from the result of the I-channel scaled data signal multiplied by a sine waveform to generate a Q-channel frequency shifted data signal. In the exemplary embodiment, the sine waveform and the cosine waveform each have a frequency of one fourth the sampling frequency.

The step of filtering the frequency shifted scaled data signal may include 16-tap finite impulse response filtering utilizing a set of predetermined filter coefficients for each of the I-channel and the Q-channel. Each set of filter coefficients includes nine non-zero coefficients with each coefficient being a 10-bit coefficient.

Brief Description of the Drawings

Figure 1 is a diagram of a complex modulation constellation useful in the practice of the present invention;

Figure 2 is a block diagram of a I/Q modulation circuit in accordance with this invention; and

Figure 3 is a block diagram of a digital filter useful in implementing an embodiment of this invention.

Description of the Preferred Embodiments

The present invention will now be described in detail with reference to the drawings. In the drawings, like reference numerals are used to refer to like elements throughout.

Referring to Figure 2, a first embodiment of a transmitter circuit 20 for I/Q modulation, frequency translation, and pulse shaping is shown. Transmitter circuit 20 includes mapper 22 which will typically include a look up table for generating each of an I-channel and a Q-channel baud rate data signal using techniques known in the art. In the exemplary embodiment, each data signal is a 7-bit value and the data is either at a 2MHz or 4MHz baud rate. However, both the 2Mbaud and the 4Mbaud data are represented by a data signal comprising a series of data values clocked at 4MHz, every other data value being a zero for the 2Mbaud data. The I-channel data signal and the Q-channel data signal are each input to a pre-scaler 24(I) and 24(Q) respectively. Prescaler 24(I) multiples the I-channel data signal by a scaler value from a multiplexer 26 and similarly, prescaler 24(Q) multiplies the Q-channel data signal by a scaler value from the multiplexer 26. The multiplexer 26 selects between scaler values of 1 and 2/3 based on an input baud rate signal. When the baud rate is 2MHz the selected scaler value is 1 and when the baud rate is 4MHz, the selected scaler value is 2/3. The purpose of scaling the I-channel data signal and the Q-channel data signal is to assure that the total signal strength remains within the required range independent of the baud rate.

The outputs of the pre-scalers 24(I) and 24(Q) are input to a complex mixer 28. The complex mixer 28 includes a first multiplier 30 and a second multiplier 32 each multiplying the I-channel data signal by a 1MHz sine waveform and a 1MHz cosine waveform respectively. A third multiplier 34 and a fourth multiplier 36 each multiply the Q-channel data signal by the 1MHz sine waveform and a 1MHz cosine waveform respectively. An I-channel summer 38 subtracts the result of the third multiplier 34 from the result of the second multiplier 32 and a Q-channel summer 40 adds the result of first multiplier 30 and the result of the fourth multiplier 36. The 1MHz sine waveform and the 1MHz cosine waveform each

have a frequency of one fourth the frequency of the data samples such that such that its digital representation consist entirely of the values of 1, 0, and -1 and thus multiplication hardware can be greatly simplified.

The I-channel output and the Q-channel output of the complex mixer 28 are input to each of each of an I-channel upsampler 42(I) and a Q-channel upsampler 42(Q) respectively which function to increase the sampling rate from 4MHz to 32 MHz by inserting sample values of zero at a 32MHz rate between the 4MHz sample values.

The 32MHz samples of each of the I-channel signal and the Q-channel signal are input to each of an I-channel pulse shaper 44(I) and a Q-channel pulse shaper 44(Q) respectively (collectively referred to as pulse shapers 44). Pulse shapers 44 are 16-tap finite impulse response (FIR) digital filters.

Referring briefly to Figure 3, a 16-tap FIR filter 44 is shown in more detail. Input port 45 of filter 44 receives each sequential sample value. In a first clock cycle, a first sample value is input to each of multiplier 46(0), operating to multiply the first sample value by a coefficient C(0), and a delay register 48(1) which operates to store the first sample value for one clock cycle. At a second clock cycle, immediately following the first clock cycle, the first sample value is released from delay register 48(1) and input to multiplier 46(1) where it is multiplied by a second coefficient C(1). Simultaneously, the first sample value is also input to a second delay register 48(2) wherein it will be stored before being input to a third multiplier 46(2) in a third clock cycle and to subsequent delay registers 48(3) to 48(15) and subsequent multipliers 46(3) to 46(15) in subsequent clock cycles in a similar manner.

Simultaneously at the second clock cycle, a second sample value at input port 45 is input to the first delay register 48(1). At each clock cycle, the results from each multiplier 46(0) to 46(15) are input to summer 50 which adds such results and generates output signal on line 52 which is a series of filtered sample values occurring at the 32MHz sampling frequency.

In the exemplary embodiment, the value for each of the 16 coefficients C(0) through C(15) is as set forth in the following table:

Coefficient	Value	Coefficient	Value
0	-0.011	8	0.924
1	0.000	9	0.000
2	0.062	10	-0.219
3	0.000	11	0.000
4	-0.219	12	0.062
5	0.000	13	0.000
6	0.924	14	-0.011
7	1.513	15	0.000

It should be appreciated that the pulse shaper 44 comprising the 16-tap FIR filter only needs to include nine multipliers as only nine of the sixteen coefficients is non-zero. Further, referring again to Figure 2, it should be appreciated that a characteristic of both the 32MHz I-channel signal and the 32MHz Q-channel signal from the complex mixer 28 is that each data value is followed by seven values of zero which are inserted by the upsampler 42(I) and 42(Q). As such, there is a maximum of only two non-zero samples that can reside in a 16-TAP filter at any particular time and therefore the pulse shaper 44 can be implemented with only two multipliers rather than the typical 16 multipliers.

The coefficients for pulse shapers 44(I) and 44(Q) are stored in two coefficient matrixes 54(I) and 54(Q). Each coefficient matrix 54(I) and 54(Q) is a 9x10 matrix which stores a single set of non-zero coefficients. Each set contains nine non-zero coefficients and each coefficient is 10 bits wide.

A summer 56 operates to subtract the result of pulse shaper 44(Q) from the result of pulse shaper 44(I) resulting in a sequence of sample values representing the I/Q amplitude modulated carrier signal. Such sequence of samples is then converted to an analog carrier signal and transmitted over a transmission medium using digital to analog techniques known to those skilled in the art.

It should be appreciated that the device and methods of this invention provide for I/Q modulation, frequency translation, upsampling, and pulse shaping requiring a significantly lower gate count resulting in significantly less complex DSP hardware than known systems. Although the invention has been shown and described with respect to certain preferred embodiments, it is obvious that

equivalents and modifications will occur to others skilled in the art upon the reading and understanding of the specification. The present invention includes all such equivalents and modifications, and is limited only by the scope of the following claims.